

1 1. A method comprising:
2 forming a buried line of a first conductive type
3 in a substrate, said buried line including a pair of more
4 lightly doped regions around a more heavily doped region;
5 creating a region of a second conductivity type
6 opposite said first conductivity type over said line; and
7 forming a phase-change material over said region.

1 2. The method of claim 1 including forming a passage
2 through a dielectric layer.

1 3. The method of claim 2 including forming a contact
2 layer under said dielectric layer and forming said passage
3 through said dielectric layer to said contact layer.

1 4. The method of claim 3 including forming the
2 phase-change material in said passage.

1 5. The method of claim 1 including forming a buried
2 line wherein said lightly doped regions reduce the reverse
3 bias leakage of said line.

1 6. The method of claim 5 including forming said more
2 lightly doped regions using ion implantation.

1 7. The method of claim 1 including forming a pair of
2 trenches on either side of said buried line.

1 8. The method of claim 1 wherein forming a buried
2 line includes forming a buried wordline.

1 9. The method of claim 1 including forming said more
2 lightly doped regions of N type material.

1 10. The method of claim 9 including forming a P type
2 region over said buried line and forming said buried line
3 in a P type substrate.

1 11. A memory cell comprising:
2 a substrate;
3 a phase-change material over said substrate;
4 a buried line of a first conductivity type in
5 said substrate, said buried line including a pair of more
6 lightly doped regions around a more heavily doped region;
7 and
8 a region of a second conductivity type opposite
9 said first conductivity type over said line and under said
10 phase-change material.

1 12. The memory cell of claim 11 including a
2 dielectric material defining a pore over the substrate,
3 said phase-change material being formed in said pore.

1 13. The memory cell of claim 12 including a contact
2 layer under said dielectric layer aligned with said pore.

1 14. The memory cell of claim 13 wherein said lightly
2 doped regions reduce the reverse bias leakage of said line.

1 15. The memory cell of claim 13 including a pair of
2 trenches on either side of said buried line.

1 16. The memory cell of claim 11 wherein said line is
2 a wordline that couples to other memory cells.

1 17. The memory cell of claim 11 wherein said lightly
2 doped regions are N-type material.

1 18. The memory cell of claim 17 wherein said lightly
2 doped regions are N- regions.

1 19. The memory cell of claim 18 wherein said
2 substrate is a P-type substrate.

1 20. The memory cell of claim 12 wherein said pore is
2 lined with a sidewall spacer.

1 21. An electronic device comprising:
2 a surface;
3 a phase-change material over said surface; and
4 a conductive line in said surface having a more
5 heavily doped region sandwiched between more lightly doped
6 regions, said conductive line providing signals to said
7 phase-change material.

1 22. The device of claim 21 wherein said phase-change
2 material forms a memory cell of a storage.

1 23. The device of claim 22 wherein said storage is
2 part of a computer.

1 24. The device of claim 22 including a processor, an
2 interface and a bus coupled to said storage.

1 25. The device of claim 22 wherein said conductive
2 line is a buried wordline.

1 26. The device of claim 25 including a conductive
2 material between said phase-change material and said
3 conductive line.

1 27. The device of claim 26 wherein said conductive
2 line is formed of a material having a first conductivity
3 type, a material of a second conductivity type being
4 defined in said surface over said conductive line.

1 28. The device of claim 27 wherein said more heavily
2 doped region is an N+ region and said more lightly doped
3 regions are N- regions.

1 29. The device of claim 21 wherein said surface
2 includes a semiconductor substrate.

1 30. The device of claim 29 including an insulator
2 material positioned over said surface and a pore being
3 formed in said insulator material, said phase-change
4 material being formed in said pore.